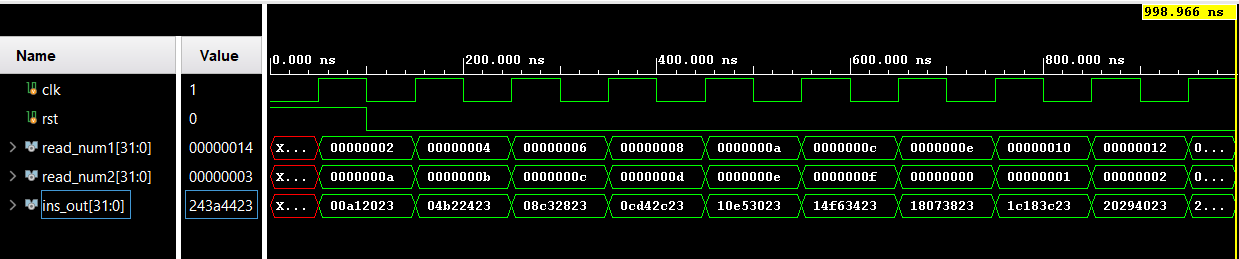
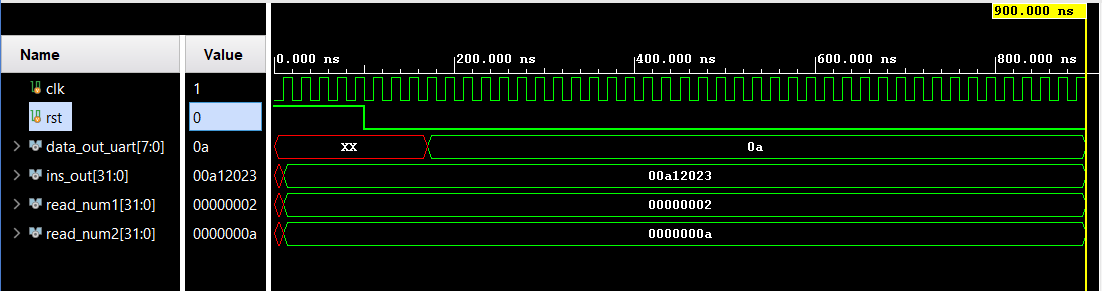
**Integration of RISC-V RV32I Core with UART Communication Using the APB Bus Interface**

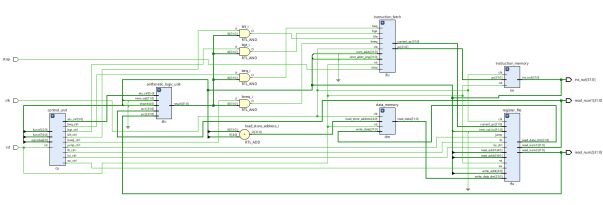
**RISC V OUTPUT WAVEFORM:**



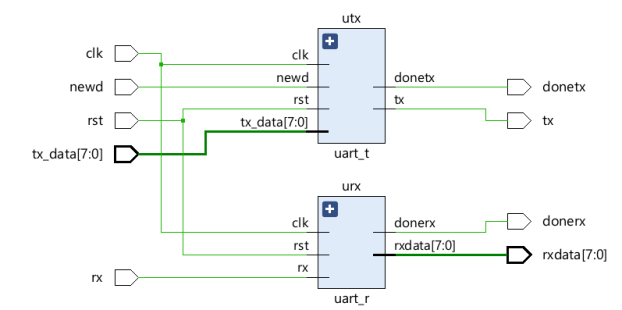
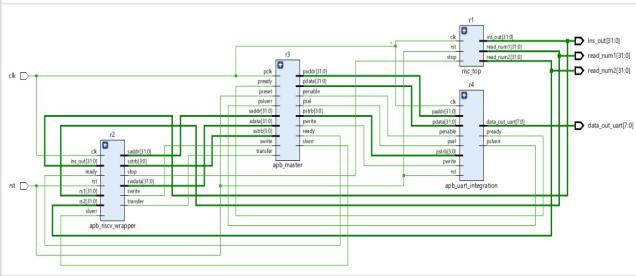
**RISC V WITH UART INTEGRATION OUTPUT WAVEFORM:**



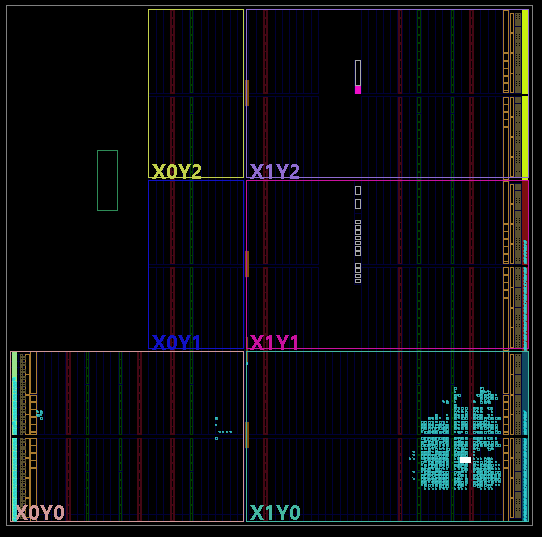
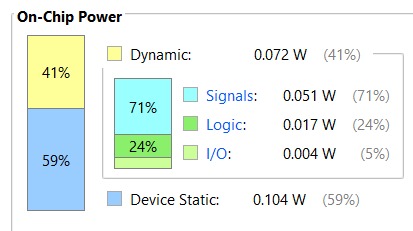
**RISC-V PROCESSOR**



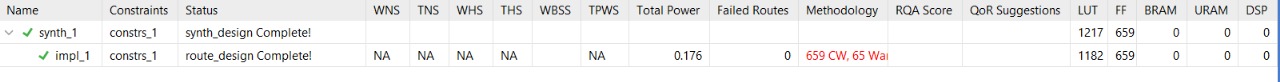
**UART TRANSMITTER & RECEIVER RISC V WITH UART INTEGRATION**

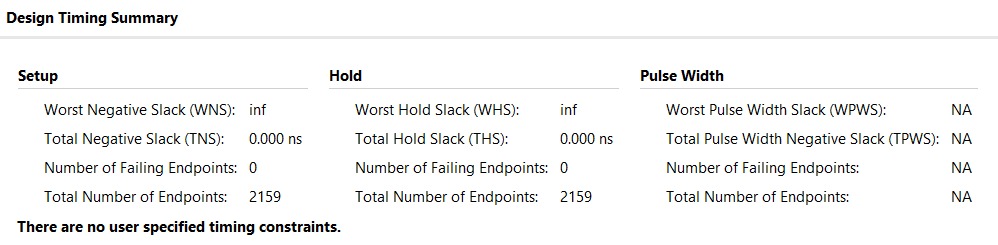
**IMPLEMENTATION ON CHIP POWER**

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**LUTS USED IN DESIGN**

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**DESIGN TIMING SUMMARY**

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